REMARKS

Claims 16-29 are pending in the application.

Claims 16-21 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Applicant requests reconsideration. Pages 2-3 of the Office Action allege that the present specification does not enable the claim 16 limitation "the first electrode not comprising the enhancement layer." Applicant notes that such feature along with its advantages and various embodiments is discussed extensively at least on page 5, line 11 to page 17, line 22 of the present specification. In particular, page 15, lines 11-12 states that a first electrode need not comprise polysilicon to accomplish surface area enhancement. Instead, as discussed on page 16, lines 1-4, the first electrode can be formed on rugged or HSG polysilicon rather than consist of the polysilicon.

Figs. 1-6 describe one of the possible embodiments wherein the first electrode need not comprise the enhancement layer. As stated on page 17, lines 1-6, even if layer 8 includes undoped polysilicon, high contact resistance may nevertheless be avoided in Fig. 6 between first electrode 10 and an underlying electrical contact in substrate 2. Thus, first electrode 10 has an enhanced surface area, yet it does not comprise undoped rugged layer 8 containing HSG polysilicon.

At least for such reasons, the present specification clearly enables the claimed capacitor construction where the first electrode does not comprise

the enhancement layer. Applicant requests withdrawal of the lack of enablement rejection in the next Office Action.

Claims 16-20 stand rejected under 35 U.S.C. 102(e) as being anticipated by Al Shareef et al. (U.S. 6,281,543B1). Applicant requests reconsideration.

Claim 16 sets forth a capacitor construction that includes, among other features, a surface area enhancement layer over a substrate, a first capacitor electrode over the enhancement layer, a capacitor dielectric layer over the first electrode, and a second capacitor electrode over the dielectric layer. The enhancement layer has an outer surface area per unit area that is greater than an inner surface area per unit area of the enhancement layer. The first electrode has an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate. The first electrode does not comprise the enhancement layer. Pages 3, 4, and 6 of the Office Action allege that HSG polysilicon layer 142 and double metal layer 144 of Al-Shareef disclose the claimed enhancement layer and first electrode. Applicant traverses on the grounds that the Office Action essentially admits that Al-Shareef fails to disclose the claimed enhancement layer. Yet, the Office maintains the rejection under 35 USC 102(e) instead of under 103, apparently because 103(c) precludes rejecting the claims over Al-Shareef which shares a common assignee with the present application.

Page 4 of the Office Action alleges that double metal layer 144 of Al-Shareef functions as a first capacitor electrode but does not comprise HSG polysilicon layer 142 as a part of such electrode. Applicant asserts that the Office's interpretation is impossible and prevents the memory cells of Al-Shareef from functioning as intended. As may be understood from column 1, lines 28-31 and column 2, lines 4-23 of Al-Shareef, those of ordinary skill clearly appreciate that any capacitor charge stored by double metal layer 144 functioning as a capacitor electrode must be electrically connected through HSG polysilicon layer 142 and conductive polysilicon material 134 to the underlying drain regions 106. This electrical connection is shown in Figs. 11-13 and the text associated therewith. Since HSG polysilicon layer 142 is positioned between double metal layer 144 and conductive polysilicon material 134, HSG polysilicon layer 142 must be conductive. Being conductive, HSG polysilicon layer 142 must be comprised by the capacitor electrode of Al-Shareef in order for a capacitor charge of such electrode to be electrically connected to drain regions 106.

In response to Applicant's assertions, the Office Action acknowledges on page 6 that Al-Shareef does not contain any disclosure of whether or not HSG polysilicon layer 142 is doped. Applicant takes that position that if HSG polysilicon layer 142 is not conductive and, thus, is not comprised by the Al-Shareef capacitor electrode, then the Al-Shareef memory cell cannot function as intended. Those of ordinary skill clearly understand this basic functional requirement of HSG polysilicon layer 142 that the Office has apparently

overlooked. Given the capacitor structure shown in Fig. 13 of Al-Shareef and the text associated therewith, it is impossible for HSG polysilicon layer 142 not to be comprised by the capacitor electrode. Any allegation otherwise contradicts the requirement that the Al-Shareef memory cell function as intended. The Office's interpretation of the properties of HSG polysilicon layer 142 cannot result in frustration of the Al-Shareef memory cell intended function.

The Office Action takes the position on page 6 that electrical connection between double metal layer 144 and drain regions 106 may occur "through the space between grains" of HSG polysilicon layer 142. Those of ordinary skill would quickly recognize this proposition as highly improbable at best. First, the Office Action does not present any evidence that it is even possible for a suitable electrical connection can be made between double metal layer 144 and drain regions 106 through "the space between grains." Double metal layer 144 is not disclosed as physically contacting drain regions 106 regardless of any alleged space between grains. Second, the Office Action does not present any evidence that a space even exists between grains of HSG polysilicon layer 142. In a conventional HSG polysilicon layer, such as shown in Fig. 10 of Al-Shareef, neighboring grains touch one another such that the grains are not spaced apart. Page 5 of the Office Action alleges that Fig. 10 shows a space between grains of HSG polysilicon layer 142. Such reliance upon Fig. 10 is misplaced since each grain is clearly shown touching adjacent grains without any space therebetween. Accordingly, Applicant

asserts that the Office's proposition for an electrical contact between double metal layer 144 and drain regions 106 is improper.

Essentially, the Office alleges that an electrical connection between double metal layer 144 and drain region 106 is inherent. "The mere fact that a certain thing may result from a given set of circumstances is not sufficient to establish inherency." In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (citations omitted) (emphasis in original); MPEP § 2112. Further, "[i]n relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis added); MPEP § 2112. Applicant asserts that the Office's technical reasoning is unreasonable and, further, that the alleged electrical connection does not necessarily result.

Since Al-Shareef cannot properly be considered to disclose the electrode as not comprising HSG polysilicon layer 142, the Office's allegation that the prior art discloses such a teaching amounts to a modification of Al-Shareef. Thus, the Office's rejection of claim 16 using Al-Shareef must be made under 35 USC 103. As such, 103(c) precludes such a rejection. Page 4 of the Office Action alleges that Al-Shareef discloses the same structure as set forth in claim 16. However, such allegation is established herein as lacking proper support in the cited art. At least for the reasons indicated

herein, Applicant asserts that Al-Shareef fails to disclose each and every limitation of claim 16.

Claims 17-20 depend from claim 16 and are not anticipated at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. For example, claim 19 sets forth that the rugged polysilicon is undoped. As may be appreciated from the discussion above regarding the deficiencies of Al-Shareef as applied to claim 16, such reference fails to disclose undoped rugged polysilicon. Also, claim 20 sets forth that the rugged polysilicon includes spaced apart grains. As also established above, Al-Shareef fails to disclose spaced apart grains and Fig. 10 expressly discloses grains that are touching instead of being spaced apart.

Applicant herein establishes adequate reasons supporting patentability of claims 16-29 and requests allowance of all pending claims in the next Office Action.

Respectfully submitted,

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